REMARKS

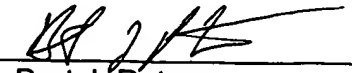
Claims 1-2, 4-7, and 9-22 are pending in this application. Claims 1 and 6 have been amended, claims 3 and 8 have been cancelled, and claims 18-22 have been added. In view of this Amendment reexamination and reconsideration are respectfully requested.

The Examiner rejected claims 1, 2, 6, 7 and 16 under 35 U.S.C. § 102(e) as being anticipated by Dhara. The remaining claims were objected as being dependent on a rejected claim. In response, Applicant has amended claims 1 and 6 by incorporating claims 3 and 8 as originally filed. These claims are now in condition for allowance as stated by the Examiner.

In addition new claims have been added. Claim 18 is similar to previous claim 9. Applicant believes the cited art does not teach or suggest the claimed invention in these new claims. The cited art does not teach or suggest an integrated transmitter circuit having a sampling section operable to sample a plurality of selected bits in the output bitstream to determine a state of each of said selected bits and an error detecting section operable to determine if the selected bits conforms to an expected state. Consideration of the newly added claims is requested.

Respectfully submitted,

Texas Instruments Incorporated

By 

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